AMENDMENTS TO THE CLAIMS:

Please cancel claims 1-15 without prejudice or disclaimer of the subject matter thereof, and add new claims 16-27, as indicated in the following listing of claims, which replaces all prior versions and listings of claims in the application:

Claims 1-15. (Canceled).

16. (New) A method of simulating an operation of memory, comprising:

supplying a memory address, which includes a first bit set for specifying a location to be accessed in a memory model and a second bit set for specifying an error address on which an error is to be generated, to the memory model describing the operation of the memory, thereby to simulate a read/write operation corresponding to the location specified by the first bit set of the memory address; and

generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set.

17. (New) The method according to claim 16, wherein the second bit set of the memory address includes error address information for specifying the error address and error mode information for specifying a content of error generation, and the generating includes:

detecting whether a value of the first bit set of the memory address and a value of the error address coincide with each other; and

reversing at least one bit of one of the write data and the read data in accordance with the error mode information when the value of the first bit set of the memory address and the value of the error address coincide with each other.

18. (New) The method according to claim 16, wherein the memory model describes an operation of a nonvolatile semiconductor memory to which write data and an error correction code thereof are written in units of data size so as to correspond to each other, and the method further comprises simulating an error correcting operation of a memory controller for controlling the nonvolatile semiconductor memory, based on the read data and the error correction code, using an LSI model describing an operation of the memory controller.

19. (New) The method according to claim 18, wherein the generating includes a first error mode for changing one of the write data to be written to the memory model and the read data read therefrom by the number of error correctable bits using the error correction code and a second error mode for changing one of the write data and the read data by the number of bits exceeding the number of error correctable bits, one of the first error mode and the second error mode being chosen in accordance with the value of the second bit set of the memory address.

20. (New) A system for simulating an operation of a memory comprising:

means for supplying a memory address, which includes a first bit set for specifying a location to be accessed in a memory model and a second bit set for specifying an error address on which an error is to be generated, to the memory model

describing the operation of the memory, thereby to simulate a read/write operation corresponding to the location specified by the first bit set of the memory address, and

means for generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set.

21. (New) The system according to claim 20, wherein the second bit set of the memory address includes error address information for specifying the error address and error mode information for specifying a content of error generation, and the error generating means includes:

means for detecting whether a value of the first bit set of the memory address and a value of the error address coincide with each other, and

means for reversing at least one bit of one of the write data and the read data in accordance with the error mode information when the value of the first bit set of the memory address and the value of the error address coincide with each other.

22. (New) The system according to claim 20, wherein the memory model describes an operation of a nonvolatile semiconductor memory to which write data and an error correction code thereof are written in units of data size so as to correspond to each other, and the system further comprises means for simulating an error correcting operation of a memory controller for controlling the nonvolatile semiconductor memory, based on the read data read from the memory model and the error correction code, using an LSI model describing an operation of the memory controller.

23. (New) The system according to claim 22, wherein the error generating means includes a first error mode for changing one of the write data to be written to the memory model and the read data read therefrom by the number of error correctable bits using the error correction code and a second error mode for changing one of the write data and the read data by the number of bits exceeding the number of error correctable bits, one of the first error mode and the second error mode being chosen in accordance with the value of the second bit set of the memory address.

24. (New) A program which is stored in a computer readable media and simulates an operation of a memory, the program comprising:

first code means for supplying a memory address, which includes a first bit set for specifying a location to be accessed in a memory model and a second bit set for specifying an error address on which an error is to be generated, to the memory model describing the operation of the memory, thereby to simulate a read/write operation corresponding to the location specified by the first bit set of the memory address; and

second code means for generating an error in the read/write operation of the memory model by changing one of write data to be written to the memory model and read data read therefrom to error data, when a value of the first bit set coincides with a value of the error address specified by the second bit set.

25. (New) The program according to claim 24, wherein the second bit set of the memory address includes error address information for specifying the error address and error mode information for specifying a content of error generation, and the second code means includes:

means for detecting whether a value of the first bit set of the memory address and a value of the error address coincide with each other; and

means for reversing at least one bit of one of the write data and the read data in accordance with the error mode information when the value of the first bit set of the memory address and the value of the error address coincide with each other.

26. (New) The program according to claim 24, wherein the memory model describes an operation of a nonvolatile semiconductor memory to which write data and an error correction code thereof are written in units of data size so as to correspond to each other, and the program further comprises third code means for simulating an error correcting operation of a memory controller for controlling the nonvolatile semiconductor memory, based on the read data read from the memory model and the error correction code, using an LSI model describing an operation of the memory controller.

27. (New) The program according to claim 26, wherein the second code means includes a first error mode for changing one of the write data to be written to the memory model and the read data read therefrom by the number of error correctable bits using the error correction code and a second error mode for changing one of the write data and the read data by the number of bits exceeding the number of error correctable bits, one of the first error mode and the second error mode being chosen in accordance with the value of the second bit set of the memory address.